IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent application of	:	
Yong-Joon CHO et al.	:	Group Art Unit: 1792
Application No. 10/712,052	:	Examiner: Shamim AHMED
Filed: November 14, 2003	:	Confirmation No.: 9035

METHOD OF FORMING A CONTACT IN A SEMICONDUCTOR DEVICE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

U.S. Patent and Trademark Office
e-FILING
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

In response to the Office Action made final dated March 3, 2008, and the Advisory Action dated June 9, 2008, applicants request review of the final rejections in the above-identified application. No amendments are being filed with this request. This paper is being filed with a Notice of Appeal.

This review is requested for the reasons stated on the attached sheets.

I. Applicants Submit that the Examiner Has Made Clear Errors in the Rejections of Claims 1-3, 5, 8-10, and 12-21.

Claim 21

Claim 21 recites "forming **a gate** on a device formation region of a semiconductor substrate, **and forming source and drain regions** in the device formation region of the semiconductor substrate **adjacent respective sides of the gate**." Claim 21 also recites "performing the dry etching process to etch the first interlayer insulating film until portions of the etch stop layer disposed over **the source region**, **the drain region** and the first and second sidewall spacers are exposed."

In the Office Action dated March 3, 2008 (hereafter "the Office Action"), claim 21 was rejected under 35 U.S.C. § 103 over a proposed combination of U.S. Patent No. 5,926,710 to Tseng and U.S. Patent No. 6,010,931 to Sun et al. (hereafter "Sun"). The Office Action relies on Sun in attempting to show "performing the dry etching process to etch the first interlayer insulating film until portions of the etch stop layer disposed over the source region, the drain region and the first and second sidewall spacers are exposed," as recited in claim 21.

Referring to remarks made by applicants in a response filed December 5, 2007, the Office Action states

> In response to the argument, examiner states that the argument is not persuasive because portions of source/drain regions (80 and 84) are exposed after etching even though the source/drain region 82 is covered with the insulating layer 96 and also the spacer 64 is exposed after the etching process (figure 8).

However, applicants submit that Tseng and Sun, as relied upon in the Office Action, fail to show "performing the dry etching process to etch the first interlayer insulating film until portions of the etch stop layer disposed over **the source region**, **the drain region** and the first and second sidewall spacers are exposed," as recited in claim 21, at least because source/drain regions 80 and 84 of FIG. 8 of Sun cannot be characterized as the source region and the drain region recited in claim 21. FIG. 8 of Sun is reproduced below.

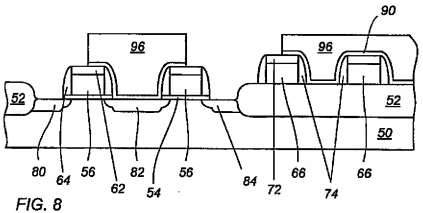

FIG. 8

Claim 21 recites "forming **a gate**," and recites "**forming source and drain regions** in the device formation region of the semiconductor substrate **adjacent respective sides of the gate**." However, applicants submit that source/drain regions 80 and 84 of FIG. 8 of Sun cannot be characterized as the source region and the drain region recited in claim 21 at least because source/drain regions 80 and 84 are not formed adjacent respective sides of **a gate**. Applicants submit that FIG. 8 of Sun shows that source/drain regions 80 and 84 are formed adjacent to different gate electrodes 56 of Sun.

Thus, applicants submit that Tseng and Sun, as relied upon in the Office Action, fail to show "performing the dry etching process to etch the first interlayer insulating film until portions of the etch stop layer disposed over **the source region**, **the drain region** and the first and second sidewall spacers are exposed," as recited in claim 21, at least because source/drain regions 80 and 84 are not formed adjacent respective sides of **a gate**. The Office Action seems to characterize etch stop layer 90 of Sun as the etch stop layer recited in claim 21. However, applicants submit that Sun, as relied upon in the Office Action, fails to disclose, for example, exposing portions of etch stop layer 90 disposed over a source region and a drain region disposed adjacent respective sides of a gate at least because source/drain regions 80 and 84 of FIG. 8 of Sun are not formed adjacent respective sides of a gate.

In addition, claim 21 also recites "wet etching the buffer layer and the etch stop layer to expose **the source region**, **the drain region** and the first and second sidewall spacers," as recited in claim 21. The Office Action states that

> Sun also teaches plasma etching the etch stop layer 90 and alternatively wet etching the etch stop layer from within the openings in the dielectric layer. The latter etch step reads on wet etching the buffer layer and the etch stop layer. Sun further teaches after the etching steps not only the surfaces of **the source, drain regions 80, 84** but also the spacer 64 are exposed (column 9, lines 5-8) which thereby reads on, wet etching the buffer layer and the etch stop layer to expose the source region, the drain region and the sidewall spacers.

(Emphasis added). However, applicants again submit that source/drain regions 80 and 84 of FIG. 8 of Sun cannot be characterized as the source region and the drain region recited in claim 21 at least because source/drain regions 80 and 84 are not formed adjacent respective sides of **a gate**. Thus, applicants submit that Tseng and Sun, as relied upon in the Office Action, fail to disclose "wet etching the buffer layer and the etch stop layer to expose **the source region**, **the drain region** and the first and second sidewall spacers," as recited in claim 21, at least because source/drain regions 80 and 84 are not formed adjacent respective sides of **a gate**.

Thus, for at least the reasons set forth above, applicants submit that the stated rejection of claim 21 is improper and request that the stated rejection of claim 21 be withdrawn.

Claims 1-3, 5, 8-10, and 12-20

Similar to claim 21, claim 1 recites

> forming **a gate** on a device formation region of a semiconductor substrate, and **forming source and drain regions** in the device formation region of the semiconductor substrate **adjacent respective sides of the gate**, . . .
>
> dry etching the first interlayer insulating film until portions of the etch stop layer disposed over **the source region**, **the drain region** and the sidewall spacers are exposed to form self-aligned contact holes in the first interlayer insulating film over the source region and the drain region, respectively;
>
> wet etching the etch stop layer to remove the portions of the etch stop layer disposed over **the source region**, **the drain region** and the sidewall spacers.

In the Office Action, claim 1 was rejected under 35 U.S.C. § 103 over a proposed combination of Tseng, Sun, and U.S. Patent No. 6,806,549 to Tomita. However, applicants submit that Tseng and Sun, as relied upon in the Office Action, fail to meet all of the features of claim 1 at least for reasons similar to those set forth above with regard to claim 21. Additionally, applicants submit that Tomita, as relied upon in

the Office Action, fails to cure all of the deficiencies of the combination of Tseng and Sun proposed in the Office Action.

Thus, at least for reasons similar to those set forth above with regard to claim 21, applicants submit that the stated rejection of claim 1 is improper and requests that the stated rejections of claim 1 and its dependencies (which are claims 2-3, 5, 8-10, and 12-20) be withdrawn.

CONCLUSION

For at least the reasons set forth above, applicants respectfully request that the rejections of claims 1-3, 5, 8-10, and 12-21 be withdrawn and that the application be returned to the Examiner for further prosecution.

Respectfully submitted,
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